

A new digital architecture for dependable, ultra-low-power biomedical implants

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During the last decade, an unprecedented market turn towards portable, embedded systems has been witnessed. Mobile telephony, ubiquitous computing (e.g. multimedia applications) and other fields have created a need for building portable devices of low power consumption. Moreover, the fields of wireless sensor networks and biomedical implants – such as pacemakers – have tightened the power budget further and have added extra requirements for dependable design. Anticipated is also the need for systems which can be built in part or in whole from reusable components, say I.P. (Intellectual-Property) cores.

The realization of portable, high-performance and at the same time low-power consuming systems has been greatly facilitated by the recent, phenomenal advances in CMOS technology, featuring ultra-low-power transistors of miniature size, which has redefined what is "feasible" and what is not. Thus, new design approaches can now be investigated for developing new generations of low-power, embedded devices.

Our research is focused on **biomedical, microelectronic implants** which impose *ultra-low-power* and *high-reliability* requirements. Moreover, their extremely high design cost calls for a *generic design approach*. In this way, different implantable systems can be developed based on an initial, modular design, effectively diminishing recurring development costs and reducing time-to-market. We work on developing a *digital architecture* for such systems which will take into consideration all above requirements. The architecture will be generic in nature so that it can be (re)used for a wide range of different biomedical applications (e.g. glucose-sensing, temperature/intra-cranial pressure monitoring etc.) and potentially for wireless-sensor-network applications. It will do so by allowing a large gamut of different sensors and/or actuators to be interfaced and controlled by it. Moreover, the architecture will be actively designed for dependability by inherently supporting dynamic error detection, fault isolation and correction. Lastly, the architecture will be minimalistic in nature (low bit count, small instruction set) so as to implement all above features while at the same time adhering to a strict ultra-low-power consumption requirement ($<100 \mu\text{W}$).